WHAT IS CLAIMED IS:

1. A method of manufacturing a semiconductor device, comprising the steps of:

(a) mounting a plurality of semiconductor chips on a first surface of a first substrate;

(b) setting the first substrate with the plural semiconductor chips mounted thereon into a mold so that a second surface of the first substrate opposite to the first surface faces a lower mold half of the mold and so that the plural semiconductor chips on the first surface are received into one cavity of the mold;

(c) sealing the plural semiconductor chips with resin in block to form a seal member while interposing a film between an upper mold half of the mold and the first surface of the first substrate;

(d) releasing the seal member from the mold with use of the film; and

(e) cutting the first substrate and the seal member into individual semiconductor devices.

2. The method according to claim 1, wherein, in the sealing step with resin, the film is vacuum-chucked and the second surface of the first substrate is vacuum-chucked to the lower mold half of the mold.

3. The method according to claim 1, wherein a first area with a group of semiconductor device forming areas formed

therein and a second area located outside the first area are arranged on each of the first and second surfaces of the first substrate, and a reinforcing pattern is formed in the second area.

4. The method according to claim 3, wherein the reinforcing pattern is formed and arranged as divided patterns.

5. The method according to claim 4, wherein the divided reinforcing patterns are arranged in the semiconductor device forming areas respectively.

6. The method according to any of claims 3 to 5, wherein out of the reinforcing patterns, a predetermined reinforcing pattern has a pattern structure capable of expansion and contraction along the first and second surfaces.

7. The method according to claim 6, wherein the predetermined reinforcing pattern comprises a plurality of first patterns separated from each other, the first patterns being adjacent to each other in a transverse direction thereof and displaced from each other in a longitudinal direction thereof.

8. The method according to claim 6, wherein the predetermined reinforcing pattern comprises tile-like patterns.

9. The method according to claim 1, wherein on the first

and second surfaces of the first substrate are arranged a conductor pattern for wiring and a conductor pattern for dummy, the conductor pattern for dummy being arranged in an area other than the area where the conductor pattern for wiring is arranged.

10. The method according to claim 9, wherein the conductor pattern for dummy is arranged in a divided manner.

11. The method according to claim 9, wherein the conductor pattern for dummy is arranged at a center of each of plural semiconductor device forming areas formed on one or both of the first and second surfaces.

12. The method according to claim 9, wherein the conductor patterns are arranged on the first and second surfaces so as to approach each other.

13. The method according to claim 1, wherein an insulating film which covers the first and second surfaces of the first substrate is provided also in an area free of any conductor pattern for wiring.

14. The method according to claim 13, wherein the insulating film is formed on each of the first and second surfaces so that the insulating films coated on the first and second surfaces approach each other.

15. The method according to claim 1, wherein a hole extending through both the first and second surfaces is formed in each of plural semiconductor device forming areas

on the first substrate, and a dam area is provided around the hole formed in the first surface, the dam area being formed by removing part of an insulating film.

16. A method of manufacturing a semiconductor device, comprising the steps of:

(a) mounting a plurality of semiconductor chips on a first surface of a first substrate;

(b) setting the first substrate with the plural semiconductor chips mounted thereon into a mold so that a second surface of the first substrate opposite to the first surface faces a lower mold half of the mold;

(c) sealing the plural semiconductor chips with resin in block to form a seal member while allowing the second surface of the first substrate to be vacuum-chucked to the lower mold half of the mold; and

(d) cutting the first substrate and the sealing member and taking out individual semiconductor devices.

17. The method according to claim 16, further including a step of heating the first substrate for a predetermined time after the step (b) and before the step (c).

18. The method according to claim 16, further including, after the step (c) and before the step (d), a step of bonding a plurality of bumps respectively to a plurality of conductor patterns for wiring simultaneously, the conductor patterns for wiring being formed in a plurality of

semiconductor device forming areas arranged on the second surface of the first substrate.

19. The method according to claim 16, wherein a first area with a group of semiconductor device forming areas formed therein and a second area located outside the first area are arranged on each of the first and second surfaces of the first substrate, and a reinforcing pattern is formed in the second area.

20. The method according to claim 19, wherein the reinforcing pattern is formed and arranged as divided patterns.

21. The method according to claim 20, wherein the divided reinforcing patterns are arranged in the semiconductor device forming areas respectively.

22. The method according to any of claims 19 to 21, wherein out of the reinforcing patterns, a predetermined reinforcing pattern has a pattern structure capable of expansion and contraction along the first and second surfaces.

23. The method according to claim 22, wherein the predetermined reinforcing pattern comprises a plurality of first patterns separated from each other, the first patterns being adjacent to each other in a transverse direction thereof and displaced from each other in a longitudinal direction thereof.

24. The method according to claim 22, wherein the predetermined reinforcing pattern comprises tile-like patterns.

25. The method according to claim 16, wherein on the first and second surfaces of the first substrate are arranged a conductor pattern for wiring and a conductor pattern for dummy, the conductor pattern for dummy being arranged in an area other than the area where the conductor pattern for wiring is arranged.

26. The method according to claim 25, wherein the conductor pattern for dummy is arranged in a divided manner.

27. The method according to claim 25, wherein the conductor pattern for dummy is arranged at a center of each of plural semiconductor device forming areas on one or both of the first and second surfaces.

28. The method according to claim 25, wherein the conductor patterns are arranged on the first and second surfaces so as to approach each other.

29. The method according to claim 16, wherein an insulating film which covers the first and second surfaces of the first substrate is provided also in an area free of any conductor pattern for wiring.

30. The method according to claim 29, wherein the insulating film is formed on each of the first and second surfaces so that the insulating films coated on the first

and second surfaces approach each other.

31. The method according to claim 16, wherein a hole extending through both the first and second surfaces is formed in each of plural semiconductor device forming areas on the first substrate, and a dam area is provided around the hole formed in the first surface, the dam area being formed by removing part of an insulating film.

32. A method of manufacturing a semiconductor device, comprising the steps of:

(a) mounting a plurality of semiconductor chips on a first surface of a first substrate;

(b) setting the first substrate with the plural semiconductor chips mounted thereon into a mold so that a second surface of the first substrate opposite to the first surface faces a lower mold half of the mold;

(c) interposing a film between an upper mold half of the mold and the first surface of the first substrate, allowing the film to be vacuum-chucked to the upper mold half, further allowing the second surface of the first substrate to be vacuum-chucked to the lower mold half of the mold, and in this state sealing the plural semiconductor chips with resin in block to form a seal member;

(d) releasing the seal member from the mold with use of the film; and

(e) cutting the first substrate and the seal member and

taking out individual semiconductor devices.

33. A method of manufacturing a semiconductor device, comprising the steps of:

(a) mounting a plurality of semiconductor chips on a first surface of a first substrate;

(b) setting the first substrate with the plural semiconductor chips mounted thereon into a mold so that a second surface of the first substrate opposite to the first surface faces a lower mold half of the mold;

(c) pouring a sealing resin into a cavity of the mold to form a seal member which seals the plural semiconductor chips together;

(d) releasing the seal member from the mold; and

(e) cutting the first substrate and the seal member and taking out individual semiconductor devices;

wherein a first area with a group of semiconductor device forming areas formed therein and a second area located outside the first area are arranged on each of the first and second surfaces of the first substrate, and plurally divided reinforcing patterns are arranged in the second area.

34. The method according to claim 33, wherein the divided reinforcing patterns are arranged respectively for the semiconductor device forming areas.

35. The method according to claim 33 or 34, wherein out of

the reinforcing patterns, a predetermined reinforcing pattern has a pattern structure capable of expansion and contraction along the first and second surfaces.

36. The method according to claim 35, wherein the predetermined reinforcing pattern comprises a plurality of first patterns separated from each other, the first patterns being adjacent to each other in a transverse direction thereof and displaced from each other in a longitudinal direction thereof.

37. The method according to claim 35, wherein the predetermined reinforcing pattern comprises tile-like patterns.

38. The method according to claim 32, wherein on the first and second surfaces of the first substrate are arranged a conductor pattern for wiring and a conductor pattern for dummy, the conductor pattern for dummy being arranged in an area other than the area where the conductor pattern for wiring is arranged.

39. The method according to claim 38, wherein the conductor pattern for dummy is arranged in a divided manner.

40. The method according to claim 38, wherein the conductor pattern for dummy is arranged at a center of each of plural semiconductor device forming areas formed on one or both of the first and second surfaces.

41. The method according to claim 41, wherein the

conductor patterns are arranged on the first and second surfaces so as to approach each other.

42. The method according to claim 33, wherein an insulating film which covers the first and second surfaces of the first substrate is provided also in an area free of any conductor pattern for wiring.

43. The method according to claim 33, wherein the insulating film is formed on each of the first and second surfaces so that the insulating films coated on the first and second surfaces approach each other.

44. The method according to claim 33, wherein a hole extending through both the first and second surfaces is formed in each of plural semiconductor device forming areas on the first substrate, and a dam area is provided around the hole formed in the first surface, the dam area being formed by removing part of an insulating film.

45. The method according to claim 33, further including, after the step (d) and before the step (e), a step of bonding a plurality of bumps respectively to a plurality of conductor patters for wiring simultaneously, the conductor patterns being arranged on the second surface of the first substrate.

46. A semiconductor device in which a semiconductor chip mounted on a first surface of a first substrate is sealed with a seal member, wherein a conductor pattern for wiring

and a conductor pattern for dummy are formed on each of the first surface of the first substrate and a second surface of the first substrate opposite to the first surface, the conductor pattern for dummy being arranged in an area other than the area where the conductor pattern for wiring is arranged.

47. The semiconductor device according to claim 46, wherein the conductor pattern for dummy is arranged in a divided manner.

48. The semiconductor device according to claim 46, wherein the conductor pattern for dummy is arranged at a center of each of plural semiconductor device forming areas formed on one or both of the first and second surfaces.

49. The semiconductor device according to claim 46, wherein the conductor patterns are arranged on each of the first and second surfaces so as to approach each other.

50. The semiconductor device according to claim 46, wherein an insulating film which covers the first and second surfaces of the first substrate is provided also in an area free of any conductor pattern for wiring.

51. The semiconductor device according to claim 46, wherein an insulating film is formed on each of the first and second surfaces so as to approach each other.

52. The semiconductor device according to claim 46, wherein a hole extending through both the first and second

surfaces of the first substrate is formed in each of plural semiconductor device forming areas on the first substrate, and a dam area is provided around the hole formed in the first surface, the dam area being formed by removing part of an insulating film.

53. The semiconductor device according to claim 46, wherein a bump electrode is formed in the conductor pattern for wiring on the second surface.

54. A semiconductor device in which a semiconductor chip mounted on a first surface of a first substrate is sealed with a seal member, wherein an insulating film which covers each of the first surface and a second surface of the first substrate is provided also in an area free of any conductor pattern for wiring.

55. A semiconductor device in which a semiconductor chip mounted on a first surface of a first substrate is seated with a seal member, wherein an insulating film is formed on each of the first surface and a second surface of the first substrate so that the insulating films coated on the first and second surfaces approach each other.

56. The semiconductor device according to any of claims 46 to 55, wherein the first substrate is mainly formed of the same type of an insulating material as that of a second substrate on which the first substrate is mounted.